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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,182	09/10/2003	Dean D. Gans	MICS:0056-1/FLE 00-0301.0	7491

7590 05/25/2005

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EXAMINER	
NGUYEN, VIET Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/659,182	GANS ET AL.
	Examiner	Art Unit
	Viet Q. Nguyen	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Response filed on 3/14/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-16 and 22-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16* is/are allowed.

6)☒ Claim(s) *22 and 27-31* is/are rejected.

7)☒ Claim(s) *23-26,32 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The applicant's response filed on 4/14/2005 has been entered.

In response to the applicant's remarks, the last office action is now withdrawn and it is replaced with this office action since only the claims are **14-16 and 22-33** are pending as correctly pointed out by the applicant. That inadvertent error is regretted.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **22, 27-29 and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nakamura (6,856,544 B2).**

Nakamura (see Fig. 1) shows a memory cell array and associated circuitry used in programming and/or testing such cell array.

Regarding claim **22, 27 & 31**, col.10 (lines 35-47) stated that a plurality of blocks can be selected (at the same time) and a "1" data ***can be written simultaneously to all blocks at the same time***, and col. 10 (lines 61-65) stated that the time required for ***testing*** can be greatly reduced, thus obviously also suggest that "***simultaneously writing to each block during the burn-in testing***" is also possible as well.

Regarding claim **27**, col.12 discussed the use of external command signals in selecting the particular memory blocks during writing and/or testing.

Regarding claims **28 & 29**, Fig. 1 shows that external addresses from eth address buffer (104) can be combined ***internally*** and the logical device (i.e., row & column decoders) are also located internally with respect the memory device as claimed.

It is noted that both claims call for the use of an **SRAM** device while Nakamura device is related to **NAND** cell device. However, Nakamura (see col. 15, lines 16-19) specifically stated that "the present invention can be applied with other devices such as DRAM's, **SRAM's** or the like", thus obviously imply that his programming method could be similarly used for all SRAM devices (like claims 22 & 27) as well.

3. Claims **22, 27-29 and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanzawa et al (6,072,719).**

Tanzawa et al (see Fig. 1) shows a memory cell array and associated circuitry used in programming and/or testing such cell array.

Regarding claim **22, 27 & 31**, col.9 and 10 stated that a plurality of blocks can be selected (at the same time) and a "1" or a "0" data ***can be written simultaneously to all blocks at the same time***, and col. 10 (lines 35-37) stated that the time required for ***testing*** can be accelerated, thus obviously also

suggest that "***simultaneously writing to each block during the burn-in testing***" is possible as well.

Regarding claim **27**, cols. 9-10 discussed the use of external command signals in selecting the particular memory blocks during writing and/or testing.

Regarding claims **28 & 29**, Fig. 1 shows that external addresses from eth address buffer (12) can be combined ***internally*** and the logical device (i.e., row & column decoders 5, 9) are also located internally with respect the memory device as claimed.

It is noted that both claims call for the use of an **SRAM** device while Nakamura device is related to **NAND** cell device. However, Tanwawa et al (see col. 16, lines 23-25) specifically stated that "the present invention is not limited to nonvolatile memories, but can be applied with other devices such as DRAM's or **SRAM's...**", thus obviously imply that his programming method could be similarly used for all SRAM devices (like claims 22 & 27) as well.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims **22, 27-31** are rejected under 35 U.S.C. 102(b) as being anticipated by **Wada et al (5,301,155).**

Wada et al (see Fig.1 A) shows a memory cell array and associated circuitry used in programming and/or testing such cell array.

Regarding all these claims, col. 6 mentions the simultaneous testing of a plurality of blocks by selecting or activating a plurality of blocks using the external block selection signals (BSA1, BSA2, BSB1, BSB2) at the same time. Thus, simultaneous writing of data to each of these block at the same time is also possible and during any burn-in testing, if any, as recited.

Wada also shows that the use of multiplexer (3) and decoders (***NAND gates*** (5, 6), as claimed "internal logical device", are used to logically combine all these internal addresses signals for selecting the particular block as recited.

6. Other remaining claims **14-16, 23-26, and 32-33** contain allowable subject matter over the prior arts of record with regard to at least the claimed use "local write drivers", "first signal", 'second signal", etc., which all of these references above lack.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen
5/22/2005